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EXAMINER	
AUVE, GLENN ALLEN	

ART UNIT	PAPER NUMBER
2111	2

DATE MAILED: 03/25/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/920,246	PRIMROSE, DONALD R.	
	Examiner	Art Unit	
	Glenn A. Auve	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-12,15,16 and 20* is/are rejected.

7)☒ Claim(s) *4,13,14 and 17-19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 July 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the first interface limitation of claim 1 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 1-6 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 is rejected because it is not clear whether the first interface is for connecting to either the first bus of the first processor or the combination of the first and second buses of the second processor or if it is for connecting to the first bus of the first processor, the first bus of the second processor, or the second bus of the second processor.

Claims 2-6 are rejected because they depend on claim 1.

Claim 6 is also rejected because it is not clear what is meant by "an identified on of said first processor and said second processor" on line 2.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 11,12, and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Freidin, U.S. Pat. No. 4,967,346.

As per claim 11, Freidin shows a control interface coupled to transmit signals between a logic device and at least one of a first processor operating with a first protocol and a second processor operating with a second protocol (abstract) comprising a first signal line (17) to receive a read strobe signal and a transfer start signal; a second line (19) to receive a write strobe signal and a read/write indicator signal; first selection logic to signal a write transaction to the logic device if the control interface is coupled to the first processor and the write strobe signal is received on the second line, or the control interface is coupled to the second processor and a transfer start signal is received on the first signal line and a write transaction is indicated by the read/write indicator on the second signal line; and second selection logic to signal a read transaction to the logic device if the control interface is coupled to the first processor and the read strobe signal is received on the first line or the interface is coupled to the second processor and a transfer start signal is received on the first signal line and a read transaction is indicated by the read/write indicator on the second signal line (fig.2 and throughout col.2 which explains how the interface which is coupled to either a Motorola or Intel processor determines which type of processor is connected and how transactions are handled). Freidin shows all of the elements recited in claim 11.

As for claim 12, the argument for claim 11 applies. Freidin also shows indicator logic coupled to the first and second selection logic to identify whether the control interface is coupled to the first processor or the second processor (abstract and col. 2). Freidin shows all of the elements recited in claim 12.

As per claim 20, Freidin shows a processor comprising internal resources (12) and interface logic to selectively couple the processor to an interchangeable one of a plurality of host processors including a first processor having a first architecture type and a second processor having a second architecture type to provide a selected one of the host processors with access to the resources (fig.2,(24) and in the abstract and col. 2). Freidin shows all of the elements recited in claim 20.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-3,5-10,15, and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Freidin in view of Geldman et al., U.S. Pat. No. 5,740,466.

As per claim 1, Freidin shows switching logic (12) and a control interface (24) for coupling one of a first type of processor or a second type of processor to the switching logic device (as in the abstract and at least in col.2 and figure 2). Freidin deals with the control signals and how they are created and used depending on which type of processor is connected. Freidin does not specifically show a first interface for connection to an interchangeable one of a first bus of a first processor and a first and second bus of a second processor, a second

interface for connection to a data bus and address bus of the switching logic, and selection logic coupled to the first and second interfaces and equipped to receive a control signal identifying one of a first mode to couple the first bus of the first processor to both the data bus and address bus of the switching logic and a second mode to couple the first bus of the second processor to the data bus of the switching logic and the second bus of the second processor to the address bus of the switching logic. However, Freidin does also disclose that the processors are either a Motorola processor or an Intel processor and the interface operates with either one of them to communicate with the device 12. Geldman shows that certain Intel processors utilize a multiplexed address/data bus while certain Motorola processors use non-multiplexed address and data buses (col.4, lines 35-41). This implies that in order for Freidin's interface to operate it needs to not only properly handle the control signals but also needs to route either the multiplexed address/data bus of one processor type or non-multiplexed buses of the other processor type to the device. Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to provide an interface between either a multiplexed address/data bus or separate address and data buses of the processors and the device as indicated in Geldman in the universal interface system of Freidin in order to make it fully compatible with either type of processor.

As for claim 2, the argument for claim 1 applies. Freidin does not specifically show that the control interface operates in the first control mode with the first interface coupled to a multiplexed address/data bus of the first processor. However, as noted above, Geldman shows that a first processor type has such a multiplexed bus and therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to provide an interface between either a multiplexed address/data bus or separate address and data buses of the processors

and the device as indicated in Geldman in the universal interface system of Freidin in order to make it fully compatible with either type of processor.

As for claim 3, the argument for claim 1 applies. Freidin does not specifically show that the control interface operates in the second control mode with the first interface coupled to non-multiplexed address/data buses of the second processor. However, as noted above, Geldman shows that a second processor type has such non-multiplexed buses and therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to provide an interface between either a multiplexed address/data bus or separate address and data buses of the processors and the device as indicated in Geldman in the universal interface system of Freidin in order to make it fully compatible with either type of processor.

As for claim 5, the argument for claim 1 applies. Freidin does not specifically show a read data bus coupled to the first interface and second interface to transmit multiplexed data and address signals between the switching logic and the first processor coupled to the first interface when in the first mode and to transmit data signals between the switching logic and the second processor coupled to the first interface in the second mode. However, as noted above, Geldman shows that a second processor type has such non-multiplexed buses and therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to provide an interface between either a multiplexed address/data bus or separate address and data buses of the processors and the device as indicated in Geldman in the universal interface system of Freidin in order to make it fully compatible with either type of processor.

As for claim 6, the argument for claim 1 applies. Freidin shows that the control signal is received from an identified one of the first processor or second processor (abstract).

As per claim 7, Freidin shows an integrated circuit (12) and a control interface (24) for coupling one of a first type of processor or a second type of processor to the integrated circuit

device (as in the abstract and at least in col.2 and figure 2). Freidin deals with the control signals and how they are created and used depending on which type of processor is connected. Freidin does not specifically show a first signal path to couple a first bus of the first processor type and a second bus of the second processor type with a data bus of the integrated circuit based at least in part on an identified processor type; a second signal path to couple the first bus of the first processor with an address bus of the integrated circuit; a third signal path to couple a third bus of the second processor type with the address bus of the integrated circuit; and selection logic coupled to select between the second and third signal paths based at least in part on the processor type. However, Freidin does also disclose that the processors are either a Motorola processor or an Intel processor and the interface operates with either one of them to communicate with the device 12. Geldman shows that certain Intel processors utilize a multiplexed address/data bus while certain Motorola processors use non-multiplexed address and data buses (col.4, lines 35-41). This implies that in order for Freidin's interface to operate it needs to not only properly handle the control signals but also needs to route either the multiplexed address/data bus of one processor type or non-multiplexed buses of the other processor type to the device. Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to provide an interface between either a multiplexed address/data bus or separate address and data buses of the processors and the device as indicated in Geldman in the universal interface system of Freidin in order to make it fully compatible with either type of processor.

As for claim 8, the argument for claim 7 applies. Freidin does not specifically show that if the selection logic selects the second signal path then the third signal path is not utilized. However, Freidin does also disclose that the processors are either a Motorola processor or an Intel processor and the interface operates with either one of them to communicate with the

device 12. Geldman shows that certain Intel processors utilize a multiplexed address/data bus while certain Motorola processors use non-multiplexed address and data buses (col.4, lines 35-41). This implies that in order for Freidin's interface to operate it needs to not only properly handle the control signals but also needs to route either the multiplexed address/data bus of one processor type or non-multiplexed buses of the other processor type to the device. Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to provide an interface between either a multiplexed address/data bus or separate address and data buses of the processors and the device as indicated in Geldman in the universal interface system of Freidin in order to make it fully compatible with either type of processor and it would be implicit in such a system that if the first processor type is connected then the third signal path would not be used.

As for claim 9, the argument for claim 8 applies. Freidin shows identification logic to identify which of the first and second processor types is coupled to the control interface (abstract).

As for claim 10, the argument for claim 7 applies. Freidin does not specifically show that the first signal path transmits data signals to the integrated circuit and the second and third signal paths transport address signals to the integrated circuit. However, Freidin does also disclose that the processors are either a Motorola processor or an Intel processor and the interface operates with either one of them to communicate with the device 12. Geldman shows that certain Intel processors utilize a multiplexed address/data bus while certain Motorola processors use non-multiplexed address and data buses (col.4, lines 35-41). This implies that in order for Freidin's interface to operate it needs to not only properly handle the control signals but also needs to route either the multiplexed address/data bus of one processor type or non-multiplexed buses of the other processor type to the device. Therefore it would have been

obvious to one of ordinary skill in the art at the time of the invention to provide an interface between either a multiplexed address/data bus or separate address and data buses of the processors and the device as indicated in Geldman in the universal interface system of Freidin in order to make it fully compatible with either type of processor and it would be implicit in such a system that if the address buses of the processors are coupled to either the second or third signal path and that the data buses of the processors are coupled to the first signal path that such address and data signals would be transferred to the integrated circuit thereby.

As per claim 15, Freidin shows a second device (12) and a control interface apparatus (24) including a first interface for coupling one of a first plurality of host device (the processors) and a second interface to couple the control interface apparatus to the second device (as in the abstract and at least in col.2 and figure 2). Freidin also shows that the first interface is equipped to receive one or more control signals including read strobe and write strobe signals if the apparatus is connected to one of the plurality of host devices operating according to a first protocol and to receive one or more control signals including a transfer start signal and a read/write indicator signal if connected to one of the host devices operating according to a second protocol (abstract and col.2). Freidin deals with the control signals and how they are created and used depending on which type of processor is connected. Freidin does not specifically show that the first interface is for connection to an interchangeably receive either multiplexed address and data signals from a first bus of a first host device, or address signals from a second bus of a second host device and data signals from a third bus of the second host device. However, Freidin does also disclose that the host devices are either a Motorola processor or an Intel processor and the interface operates with either one of them to communicate with the device 12. Geldman shows that certain Intel processors utilize a multiplexed address/data bus while certain Motorola processors use non-multiplexed address

and data buses (col.4, lines 35-41). This implies that in order for Freidin's interface to operate it needs to not only properly handle the control signals but also needs to route either the multiplexed address/data bus of one processor type or non-multiplexed buses of the other processor type to the device. Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to provide an interface between either a multiplexed address/data bus or separate address and data buses of the processors and the device as indicated in Geldman in the universal interface system of Freidin in order to make it fully compatible with either type of processor.

As for claim 16, the argument for claim 15 applies. Freidin shows that the first interface is equipped to interchangeably couple the apparatus to one of a plurality of microprocessors (abstract).

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The other cited references show other systems for allowing different processor types or signaling standards to be used in the same system.

9. Claims 4,13,14, and 17-19 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

10. The following is a statement of reasons for the indication of allowable subject matter: claims 4,13, and 17 include limitations directed to providing programmable delay circuitry in the interface. These limitations are not shown by the prior art.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Glenn A. Auve whose telephone number is (703) 305-9638. The examiner can normally be reached on M-Th 8:00 AM-5:30 PM, every other Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on (703) 305-4815. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Glenn A. Auve
Primary Examiner
Art Unit 2111

gaa
March 18, 2004